SIGNAL DETECTION BY A RECEIVER IN A MULTIPLE ANTENNA TIME-DISPERSIVE SYSTEM

Technical Field

This invention relates to the art of wireless communications, and more particularly, to wireless communication systems using multiple antennas at the transmitter and multiple antennas at the receiver, so called multiple-input multiple-output (MIMO) systems.

Background of the Invention

It has previously been assumed for MIMO systems that the time dispersion between one or more of the transmit antennas and one or more of the receive antennas was negligible, i.e., the various paths were nonresolvable, as often occurs in low bandwidth systems, because the pulse width is longer than the channel time dispersion. However, it has been recognized that under typical urban (TU) conditions, i.e., the conditions of the so-called "TU" model, that the time dispersion between one or more of the transmit antennas and one or more of the receive antennas is nonnegligible. Such a non negligible time dispersion causes the various paths to interfere with each other, resulting in a bit error rate floor, i.e., minimum, and so the resulting bit error rate is unacceptable.

I. Ghauri and D. Slock have shown, in "Linear Receivers for the DS-CDMA Downlink Exploiting Orthogonality of Spreading Codes", 32nd Asilomar Conference, Nov. 1-4, 1998 pp. 650-4, that a minimum mean square error (MMSE) equalizer operating on received code division multiple access (CDMA) chips can be employed to compensate for time dispersion in a single transmit, single receive antenna system, thus reducing the bit error rate floor and improving performance.

Summary of the Invention

We have recognized, in accordance with the principles of the invention, that in a MIMO system the bit error rate floor caused by time dispersion can be reduced by employing a joint equalizer for all of the respective transmit antenna – receive antenna pairings that are possible in the MIMO system. Advantageously, the resulting joint equalization compensates not only for the impact of the channel on the transmit antenna – receive antenna pairings but also for the interference of the other transmit antennas on any given receive antenna. In a particular embodiment of the invention, the joint equalizer is a joint minimum mean square error (MMSE) equalizer, and in such an embodiment the joint

equalization outperforms simply replicating the prior art minimum mean square error (MMSE) equalizer for each transmit antenna – receive antenna pairing.

In one embodiment of the invention, which is especially useful for CDMA, after the equalization is completed the resulting chip streams, one for each transmit antenna, are despread in the conventional manner and then the resulting depread symbols may be further processed in the conventional manner. Alternatively, instead of further processing the despread symbols in the conventional manner, the despread symbols may be processed, in accordance with an aspect of the invention, so as to have their soft bits computed through the use of a posteriori probability (APP) metric. Prior to computing the soft bits, the despread symbols may be spatially whitened using a spatial whitening filter.

In another embodiment of the invention, which is also especially useful for CDMA, the equalizer is iteratively computed so that a symbol from one transmit antenna is determined during each iteration. Initially the received samples are stored in a memory. After a symbol for an antenna is determined, the received samples for each of the remaining antennas are then recomputed by subtracting out the determined symbol from the samples as they existed prior to determining the symbol. Once all the symbols for all of the transmit antennas are determined for a symbol period are determined the operation begins anew with the samples corresponding to the next symbol period.

Brief Description of the Drawing

In the drawing:

FIG. 1 shows an embodiment a multiple-input multiple-output (MIMO) wireless system in which the bit error rate floor caused by time dispersion is reduced by employing a joint minimum mean square error (MMSE) equalizer for all of the respective transmit antenna – receive antenna pairings that are possible in the MIMO system, in accordance with the principles of the invention;

FIG. 2 shows an exemplary process, in flow chart form, for the overall operation of system of FIG. 1;

FIG. 3 shows in more detail the process by which the weights employed by the joint equalizer of FIG. 1 are determined;

FIG. 4 shows another exemplary process, in flow chart form, for the overall operation of system of FIG. 1;

FIG. 5 shows another embodiment a multiple-input multiple-output (MIMO) wireless system in which the bit error rate floor caused by time dispersion is reduced by employing a joint minimum mean square error (MMSE) equalizer for all of the respective

transmit antenna – receive antenna pairings that are possible in the MIMO system, in accordance with the principles of the invention;

FIG. 6 shows a more detailed version of a buffer-subtractor of FIG. 5;

FIG. 7 shows an exemplary process, in flow chart form, for the overall operation of system of FIG. 5;

FIG. 8 shows a particular embodiment of the joint equalizer of FIG. 1, in which the equalization is performed in the discrete frequency domain, in accordance with an aspect of the invention; and

FIG. 9 shows a particular embodiment of the joint equalizer of FIG. 1, in which the equalization is calculated in the discrete frequency domain and applied in the time domain.

Detailed Description

The following merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention and are included within its spirit and scope. Furthermore, all examples and conditional language recited herein are principally intended expressly to be only for pedagogical purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

Thus, for example, it will be appreciated by those skilled in the art that any block diagrams herein represent conceptual views of illustrative circuitry embodying the principles of the invention. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable medium and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

The functions of the various elements shown in the FIGs., including any functional blocks labeled as "processors", may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of

which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor (DSP) hardware, network processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), read-only memory (ROM) for storing software, random access memory (RAM), and non-volatile storage. Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the FIGS. are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementor as more specifically understood from the context.

In the claims hereof any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements which performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The invention as defined by such claims resides in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. Applicant thus regards any means which can provide those functionalities as equivalent as those shown herein.

Software modules, or simply modules which are implied to be software, may be represented herein as any combination of flowchart elements or other elements indicating performance of process steps and/or textual description. Such modules may be executed by hardware which is expressly or implicitly shown.

Unless otherwise explicitly specified herein, the drawings are not drawn to scale.

In the description, identically numbered components within different ones of the FIGs. refer to the same components.

FIG. 1 shows an exemplary embodiment of a multiple-input multiple-output (MIMO) wireless system in which the bit error rate floor caused by time dispersion is reduced by employing a joint minimum mean square error (MMSE) equalizer for all of the respective transmit antenna – receive antenna pairings that are possible in the MIMO system, in accordance with the principles of the invention. Shown in FIG. 1 are a) transmitter 101; b) transmit antennas 103; including transmit antennas 103-1 through 103-M; c) receive antennas 105; including receive antennas 105-1 through 105-N; d) receiver front-end 107; e) joint equalizer 109; f) optional despreaders 111; g) soft bit

mapper 112, which may include optional spatial whitening filter 113; and optional a posteriori probability (APP) metric processor 115.

Transmitter 101 is a MIMO transmitter, e.g., one in which an original data stream is divided into substreams and each resulting substream is transmitted as a modulated radio signal via an individual one of transmit antennas 103. The transmitted signals pass to the receiver over a time dispersive channel such that signals from each transmit antenna 103 reach each of receive antennas 105.

Receive antennas 105 convert the radio signals impinging upon them into electrical signals, which are supplied to receiver front-end 107. Receiver front-end 107 operates conventionally to produce a stream of binary numbers representing samples of the radio signals received at antennas 105. Typically receiver front-end 107 performs radio frequency downconversion, filtering, sampling, and analog-to-digital conversion. The resulting samples are provided to joint equalizer 109.

Joint equalizer 109 compensates for the effects of the transmit signals from each of antennas 103 having passed through the channel as well as the interference that results from transmitting via multiple antennas simultaneously. The output of joint equalizer 109 is M, i.e., the number of transmit antennas, streams of corrected symbols, or in the case of CDMA, streams of corrected chips which when properly combined form symbols. Operation of joint equalizer 109 will be described more fully hereinbelow. If CDMA is employed, the output of joint equalizer 109 is supplied to optional despreaders 111, which produces symbols from the stream of chips supplied by joint equalizer 109.

The symbols produced may then be further processed in the conventional manner for a MIMO system, e.g., soft bits may be developed by soft bit mapper 112 for use in a decoder, e.g., the well known "Turbo decoder". Alternatively, the symbols may be supplied within soft bit mapper 112 to optional spatial whitening filter 113, which makes the noise equal on each branch. Note that the whitening is performed only in the space domain. If whitening is performed in the time domain some temporal dispersion will be introduced into the signal. The symbols, or whitened symbols if optional spatial whitening filter 113 is employed, may further be supplied to optional a posteriori probability (APP) metric processor 115 within soft bit mapper 112, in accordance with an aspect of the invention. APP metric processor 115 performs a particular type of mapping from symbols to soft bits. Operation of APP metric processor 115 is described more fully hereinbelow.

FIG. 2 shows an exemplary process, in flow chart form, for the overall operation of system of FIG. 1. Prior to performing the process of FIG. 2, initial values of parameters M, N, L, P, E, and d must be determined. What each of these parameters represents is listed in Table 1. Additionally, prior to performing the process of FIG. 2 it is

necessary to determine noise covariance $\mathbf{R}_{pp}$, which contains samples of the autocorrelation of the chip pulse shape *r(t)*, when CDMA is employed, or the symbol pulse shape autocorrelation, when CDMA is not employed.

Table 1 – Parameter Definitions

M	number of transmit antennas
N	number of receive antennas
L	length of the channel impulse response (chips)
P	over-sampling factor
E	length of the equalizer (chips)
d	equalizer delay (chips)
σ_n^2	power of interference + noise (RF bandwidth)
σ_x^2	power of downlink signal (RF bandwidth)
G	Number of CDMA chips per symbol

The process of FIG. 2 is executed periodically, with a periodicity that preferably does not exceed the coherence time, T_{co}, which is the time duration for which the channel properties are substantially constant. The process is entered in step 201, in which $L*P$ discrete channel estimations h_0 to h_{LP-1} are developed. The channel estimate may be obtained using any conventional technique, e.g., by using correlators tuned to the pilot channel. Each of discrete channel estimations is taken with a time spacing of the chip duration divided by P, for CDMA, or symbol duration divided by P for TDMA. Also, in step 201, the background noise plus interference power σ_n^2 and the power of the downlink from the base station to the terminal σ_x^2 are determined in the conventional manner. In step 203, the weights employed by joint equalizer 109 are determined, as will be described fully further hereinbelow.

Next, in step 205, a set of P samples from each antenna is obtained. Thereafter, in step 207, the determined weights of joint equalizer 109 are applied to the samples from each antenna by joint equalizer 109. The samples are then despread by despreader 111, if CDMA was employed, in optional step 209. In optional step 211, conventional soft mapping of the symbols to soft bits is performed, and the resulting soft bits are supplied as an output for use by a decoder. Thereafter, conditional branch point 213 tests to determine whether one coherence time has elapsed since the previous execution of step 201. If the test result in step 213 is NO, indicating that the channel is believed to still remain substantially the same as when it was last estimated, control passes to step 205,

and the process continues as described above. If the test result in step 213 is YES, indicating that sufficient time has passed such that the channel may have changed enough so as not to be considered substantially the same as when it was last estimated, control passes back to step 201 and the process continues as described above.

FIG. 3 shows in more detail the process of step 203 by which the weights employed by joint equalizer 109. Note that the process requires the use of several matrices, and the dimensions of the various matrices are given in Table 2.

Table 2

Matrix	Dimension
$\mathbf{R}_p$	$EP \times EP$
$\mathbf{R}_{pp}$	$NEP \times NEP$
$\mathbf{\Gamma}(\mathbf{h}_{n,m})$	$EP \times (E+L-1)$
$\mathbf{\Gamma}(\mathbf{H})$	$NEP \times M(E+L-1)$
$\mathbf{\Gamma}(\mathbf{H}_m)$	$NEP \times M(E+L-1)$
$\mathbf{e}_d$	$(E+L-1) \times 1$
$\mathbf{A}$	$M \times M(E+L-1)$
$\mathbf{a}_m$	$1 \times M(E+L-1)$
$\mathbf{W}$	$M \times NEP$
$\mathbf{w}_m$	$1 \times NEP$
$\mathbf{Q}$	$M \times M$

In step 301, the channel estimates h_0 to h_{LP-1} for each transmit and receive pair obtained in step 201 are arranged in a respective matrix $\mathbf{h}_{n,m}$ as shown in equation 1. In step 303, matrix convolution operator $\mathbf{\Gamma}(\mathbf{h}_{n,m})$ is then formed for each respective matrix $\mathbf{h}_{n,m}$, as shown in equation 2. Thereafter, in step 305, MIMO convolution operator $\mathbf{\Gamma}(\mathbf{H})$ is then formed from the various matrix convolution operators as shown in equation 3.

$$\mathbf{h}_{n,m} = \begin{bmatrix} h_0 & h_P & \cdots & h_{(L-1)P} \\ \vdots & \vdots & & \vdots \\ h_{P-1} & h_{2P-1} & \cdots & h_{LP-1} \end{bmatrix} \qquad \text{equation (1)}$$

$$\mathbf{\Gamma}(\mathbf{h}_{n,m}) = \begin{bmatrix} \mathbf{h}_{n,m} & \mathbf{0}_p & \cdots & \mathbf{0}_p \\ \mathbf{0}_p & & & \\ \vdots & & \ddots & \vdots \\ \mathbf{0}_p & \cdots & \mathbf{0}_p & h_{.m} \end{bmatrix} \qquad \text{equation (2)}$$

$$\mathbf{\Gamma}(\mathbf{H})=\begin{bmatrix} \mathbf{\Gamma}(\mathbf{h}_{1,1}) & \mathbf{\Gamma}(\mathbf{h}_{1,2}) & \cdots & \mathbf{\Gamma}(\mathbf{h}_{1,M}) \\ \mathbf{\Gamma}(\mathbf{h}_{2,1}) & \mathbf{\Gamma}(\mathbf{h}_{2,2}) & & \vdots \\ \vdots & & \ddots & \\ \mathbf{\Gamma}(\mathbf{h}_{N,1}) & \cdots & & \mathbf{\Gamma}(\mathbf{h}_{N,M}) \end{bmatrix} \qquad \text{equation (3)}$$

In step 307, delay vector $\mathbf{e}_d$ is formed as shown in equation 4. Delay vector $\mathbf{e}_d$ is a one dimensional vector with E+L-1 elements which are all zero except for the single value at the E+L-1-d location, which has a value of 1. A typical value for d, which is selectable by the implementor, is such that the location which has a value of 1 is at the center of the vector. The purpose of delay vector $\mathbf{e}_d$, is to impose the overall equalizer delay d onto the equalizer. Thereafter, in step 309, delay matrix **A** is computed from equation 5, in which $\mathbf{I}_M$ is an identity matrix of size $M \times M$.

$$\mathbf{e}_d = [0 \quad \cdots \quad 1 \quad 0 \quad 0] \qquad \text{equation (4)}$$

$$\mathbf{A} = \mathbf{I}_M \otimes \mathbf{e}_d \qquad \text{equation (5)}$$

Finally, in step 311, equalizer weight matrix, **W**, is computed in accordance with equation 6, in which $\mathbf{X}^{\mathrm{H}}$ means the Hermitian transpose of **X**, which is the complex conjugate transpose of the vector or matrix **X**.

$$\mathbf{W} = \mathbf{A}\,\mathbf{\Gamma}(\mathbf{H})^H \left(\mathbf{\Gamma}(\mathbf{H})^H \mathbf{\Gamma}(\mathbf{H}) + \frac{\sigma_n^2}{\sigma_x^2}\mathbf{R}_{pp} \right)^{-1} \qquad \text{equation (6)}$$

In one embodiment of the invention, execution of step 205 is such that the P samples *r* of antenna *n* are initially arranged as a vector **c** shown in equation 7, where *k* is the current received chip time index if CDMA is employed, or the symbol time index if CDMA is not employed. E consecutive in time vectors **c** for antenna *n* are then arranged as shown in equation 8, and the E consecutive in time vectors **c** for all of the N antennas are further arranged as shown in equation 9, forming a vector of received samples at time *k*.

$$\mathbf{c}_n(k)=\begin{bmatrix} r_n(kT_c) \\ r_n(kT_c+T_s) \\ \vdots \\ r_n(kT_c+(P-1)T_s) \end{bmatrix} \qquad \text{equation (7)}$$

$$\mathbf{r}_n(k)=\begin{bmatrix} \mathbf{c}_n(k) \\ \mathbf{c}_n(k-1) \\ \vdots \\ \mathbf{c}_n(k-E+1) \end{bmatrix} \qquad \text{equation (8)}$$

$$\mathbf{r}(k)=\begin{bmatrix}\mathbf{r}_1(k)\\ \mathbf{r}_2(k)\\ \vdots\\ \mathbf{r}_N(k)\end{bmatrix} \qquad \text{equation (9)}$$

The application of the determined weights by joint equalizer 109 in step 207 may be performed as shown in equation 10, where $\mathbf{y}(k)$ is a resulting vector of size $\mathrm{M}\times 1$ which contains the equalized chips if CDMA is employed, or symbols if CDMA is not employed.

$$\mathbf{y}(k)=\mathbf{W}\mathbf{r}(k) \qquad \text{equation (10)}$$

FIG. 4 shows another exemplary process, in flow chart form, for the overall operation of system of FIG. 1. The version of the process shown in FIG. 4 is similar to that shown in FIG. 2, but it is for embodiments of the invention that include optional spatial whitening filter 113 (FIG. 1) and optional a posteriori probability (APP) metric processor 115. Unless otherwise noted, all variables and parameters employed in the process of FIG. 4 are the same as described for FIG. 2. As with the process of FIG. 2, prior to performing the process of FIG. 4, initial values of parameters M, N, L, P, E, and d must be determined. Additionally, prior to performing the process of FIG. 4 it is necessary to determine $\mathbf{R}_{pp}$.

The process of FIG. 4 is executed periodically, with a periodicity that preferably does not exceed the coherence time, T_{co}, which is the time duration for which the channel properties are substantially constant. The process is entered in step 401, in which $L*P$ discrete channel estimations h_0 to h_{LP-1} are developed. Also in step 401, the background noise plus interference power σ_n^2 and the power of the downlink from the base station to the terminal σ_x^2 are determined in the conventional manner. In step 403, the weights $\mathbf{W}$ employed by joint equalizer 109 are determined, as described hereinabove. Additionally, in step 403, the effective channel matrix $\mathbf{H}_{\text{eff}}$ and, optionally, spatial whitening filter $\mathbf{Q}$ are determined, in accordance with an aspect of the invention. More specifically, $\mathbf{H}_{\text{eff}}$ is determined as shown in equation 11, and $\mathbf{Q}$ is determined as shown in equation 12.

$$\mathbf{H}_{\text{eff}}(m,n)=\mathbf{e}_n^{T}\mathbf{W}\boldsymbol{\Gamma}(\mathbf{H})\mathbf{e}_m \quad m=1:M, \quad n=1:N \qquad \text{equation (11)}$$

$$\mathbf{Q}=\left(\mathbf{W}\mathbf{W}^{H}\right)^{-1/2} \qquad \text{equation (12)}$$

Next, in step 405 a set of P samples from each antenna is obtained. Thereafter, in step 407, the determined weights of joint equalizer 109 are applied to the samples from each antenna by joint equalizer 109. The samples are then despread by despreader 111, if CDMA was employed, in optional step 409. In step 411, whitening filter $\mathbf{Q}$ is applied to

the despread, equalizer outputs of step 409. In step 413, APP softbits are computed, in accordance with an aspect of the invention, using equations 13 and 14. The softbits are the output of the process of FIG. 4, and they may be made available to a decoder, e.g., a turbo decoder.

$$L_D(x_k|y) = \log_e\left(\frac{\Pr(x_k=1|y)}{\Pr(x_k=-1|y)}\right) = \ln\left(\frac{\sum_{\hat{x},x_k=1} p(y|X=\hat{x})\prod_{j\neq k} p(X=x_j)}{\sum_{\hat{x},x_k=-1} p(y|X=\hat{x})\prod_{j\neq k} p(X=x_j)}\right) + \ln\left(\frac{p(x_k=1)}{p(x_k=-1)}\right)$$

equation 13

$$p(\mathbf{y}|X=x_k) = \left(\frac{1}{\sqrt{2\pi}\sigma}\right)^{N_r} \exp\left(-\frac{\left\|\mathbf{y}-\mathbf{H}_{eff}\hat{\mathbf{s}}\right\|^2}{2\sigma^2}\right)$$

equation 14

Thereafter, conditional branch point 415 tests to determine whether one coherence time has elapsed since the previous execution of step 401. If the test result in step 415 is NO, indicating that the channel is believed to still remain substantially the same as when it was last estimated, control passes to step 405, and the process continues as described above. If the test result in step 415 is YES, indicating that sufficient time has passed such that the channel may have changed enough so as not to be considered substantially the same as when it was last estimated, control passes back to step 401 and the process continues as described above.

FIG. 5 shows another exemplary embodiment of a multiple-input multiple-output (MIMO) wireless system in which the bit error rate floor caused by time dispersion is reduced by employing a joint minimum mean square error (MMSE) equalizer for all of the respective transmit antenna – receive antenna pairings that are possible in the MIMO system, in accordance with the principles of the invention. Shown in FIG. 5 are a) transmitter 501; b) transmit antennas 503; including transmit antennas 503-1 through 503-M; c) receive antennas 505; including receive antennas 505-1 through 505-N; d) receiver front-end processor 507; e) buffer-subtractor 521; f) joint equalizer 523; g) optional despreader 525; h) soft bit mapper 527; i) space-time regenerator 529; j) order controller 531 and k) switch 533.

Transmitter 501 is a MIMO transmitter, e.g., one in which an original data stream is divided into substreams and each resulting substream is transmitted as a modulated radio signal via an individual one of transmit antennas 503. The transmitted signals pass to the receiver over a time dispersive channel such that signals from each transmit antenna 503 reach each of receive antennas 505.

Receive antennas 505 convert the radio signals impinging upon them into electrical signals, which are supplied to receiver front-end processor 507. Receiver front-end processor 507 operates conventionally to produce a stream of binary numbers representing samples of the radio signals received at antennas 505. Typically receiver front-end processor 507 performs radio frequency downconversion, filtering, sampling, and analog-to-digital conversion. The resulting samples are provided to buffer-substractor 521.

Buffer-subtractor 521 is shown in more detail in FIG. 6. Buffer subtractor 521 includes buffer 601, memory 603, and subtractor 605. Buffer 601 stores a time consecutive set of samples from each of antennas 505 as those samples become available from front-end processor 507. Buffer 601 supplies the samples it receives from front-end processor 507 to memory 603 when an entire set is stored, i.e., the contents of buffer 601 are quickly dumped to memory 603. Once the set of samples are stored in memory 603 they may be independently accessed and sent to joint equalizer 523 (FIG. 5). Additionally, space time samples from a second input of buffer-subtractor 521 are supplied to subtractor 605. Subtractor 605 is cable of forming the difference between a specified location in memory 603 and a second input to buffer-subtractor 521. The resulting difference is stored in the specified location in memory 603.

Joint equalizer 523 performs M passes through memory 603 with a different equalizer weight $\mathbf{w}_m$ in each pass. Each weight is chosen to emphasize transmit antenna m and to suppress transmit antennas m+1 through M.

The output of joint equalizer 523 is supplied to conventional soft bit mapper 527, via optional conventional despreader 525 if CDMA is employed. The soft bits developed by soft bit mapper 527 are then supplied as an output, such as may be used by a decoder, e.g., the well known "Turbo decoder".

The same output that is supplied to conventional soft bit mapper 527 may also be supplied to space-time regenerator 529 via switch 533. Space-time regenerator 529 forms a set of time consecutive samples for each receive antenna assuming the soft symbol is correct. In other words, assuming a particular soft symbol had been the actual symbol transmitted by a particular transmit antenna, space-time regenerator 529 creates the corresponding effect that such a symbol would have caused on each of receive antennas 505 given the channel characteristics. Operation of space-time regenerator 529 will be explained more fully hereinbelow.

Order controller 531 determines, based on channel estimates, the signal from which transmit antenna will be processed at any particular time, as will be explained more fully hereinbelow.

FIG. 7 shows an exemplary process, in flow chart form, for the overall operation of system of FIG. 5 in which switch 533 is connected between despreader 525 and space-time regenerator 529. Prior to performing the process of FIG. 7, initial values of parameters *M*, *N*, *L*, *P*, *E*, and *d* must be determined. What each of these parameters represents is listed in Table 1. Additionally, prior to performing the process of FIG. 7 it is necessary to determine $\mathbf{R}_{pp}$, which is samples of the autocorrelation of the chip pulse shape *r(t)*, when CDMA is employed, or the symbol pulse shape autocorrelation, when CDMA is not employed.

The process of FIG. 7 is executed periodically, with a periodicity that preferably does not exceed the coherence time, T_{co}. The process is entered in step 701, in which *L*P* discrete channel estimations h_0 to h_{LP-1} are developed. The channel estimate may be obtained using any conventional technique, e.g., by using correlators tuned to the pilot channel. Each discrete channel estimation is taken with a time spacing of the chip duration divided by *P*, for CDMA, or symbol duration divided by *P* for TDMA. Also in step 701, the background noise plus interference power σ_n^2 and the power of the downlink from the base station to the terminal σ_x^2 are determined in the conventional manner.

In step 703, order controller 531 determines, according to equations 15 and 16, the order in which the signals from the various transmit antennas will be processed, with the signal from a respective transmit antenna being processed for each execution of joint equalizer 523. *Sort* is a function that rearranges the elements of vector **P** so that they run from largest to smallest and *order* is a list of all the antenna transmit antenna numbers as they should be processed by joint equalizer 523. It is preferable to process the so-called "strong" signals first. However, the particular characteristic, or set of characteristics, which are used to define the "strength" of a signal is at the discretion of the implementer. In the particular embodiment shown herein, estimated signal powers are employed as the strength. Further note that although herein the order for all the antennas is determined simultaneously, those of ordinary skill in the art will readily recognize that it is possible to successively determine which antenna to process.

$$P = \left\| diag\left(\mathbf{W}\,\mathbf{\Gamma}(\mathbf{H})\right)\right\|^2 \qquad \text{equation (15)}$$

$$[P', order] = sort(P) \qquad \text{equation (16)}$$

In step 705, the equalizer weights for the particular antenna currently being processed, *m*, as specified by the order, is determined according to equations 17 and 18, in which delay vector $\mathbf{a}_m$ is the m^{th} row of delay matrix **A** which was described hereinabove.

$$\mathbf{w}_m = \mathbf{a}_m \Gamma(\mathbf{H}_m)^H \left(\Gamma(\mathbf{H}_m)^H \Gamma(\mathbf{H}_m) + \frac{\sigma_n^2}{\sigma_x^2} \mathbf{R}_{pp} \right)^{-1} \quad \text{equation (17)}$$

$$\Gamma(\mathbf{H}_m) = \begin{bmatrix} \mathbf{0} & \Gamma(\mathbf{h}_{1,2}) & \mathbf{0} & \cdots \Gamma(\mathbf{h}_{1,M}) \\ \mathbf{0} & \Gamma(\mathbf{h}_{2,2}) & \mathbf{0} & \vdots \\ \vdots & \vdots & \vdots & \vdots \\ \mathbf{0} & \Gamma(\mathbf{h}_{N,2}) & \mathbf{0} & \cdots \Gamma(\mathbf{h}_{N,M}) \end{bmatrix} \quad \text{equation (18)}$$

Note that for each iteration m of equation 18, columns corresponding to order(1) through order(m-1) are set to the block zero matrix $\mathbf{0}$. Note that order is vector which contains a listing of the M antenna numbers in the order in which they will be processed. Order may be the result of the well known function sort of MatLab®. Doing so accounts for the fact that signals from transmit antennas 1 through m-1 have already been subtracted from the signal remaining to be processed for this set of samples.

Next, in step 707 a set of samples that span at least the duration of a data symbol is obtained from each receive antenna. Thereafter, in step 709, counter variable m is initialized to 1. In step 711, the weights determined for joint equalizer 523 in step 705 are applied to the samples from each receive antenna by joint equalizer 523, in accordance with equation 19.

$$y(k) = \mathbf{w}_m{}^T \mathbf{r}(k) \quad \text{equation (19)}$$

The samples are then despread by despreader 525, if CDMA was employed, in optional step 713. In optional step 715, conventional soft mapping of the symbols to soft bits is performed, and the resulting soft bits are supplied as an output for use by a decoder.

In step 717, samples are produced by space-time regenerator 529 according to equations 20 and 21.

$$\hat{\mathbf{x}}_m(k) = \hat{d}_m(k) \begin{bmatrix} s(kG) \\ s(kG+1) \\ \vdots \\ s(kG+G-1) \end{bmatrix} \quad \text{equation (20)}$$

$$\mathbf{y}_m(k) = \begin{bmatrix} \Gamma(\mathbf{h}_{1,m}) \\ \Gamma(\mathbf{h}_{2,m}) \\ \vdots \\ \Gamma(\mathbf{h}_{N,m}) \end{bmatrix} \hat{\mathbf{x}}_m(k) \quad \text{equation (21)}$$

In step 719 the output of space-time regenerator 529 is subtracted from the contents of memory 603 (FIG. 6), as shown by equation 22.

$$\mathbf{r}(k) = \mathbf{r}(k) - \mathbf{y}_m(k) \quad \text{equation (22)}$$

Thereafter, conditional branch point 721 tests to determine if *m* is equal to *M*. If the test result in step 721 is NO, indicating that not all of the transmit antennas have yet had their signal contribution processed, *m* is incremented in step 723. Thereafter, control passes back to step 711 and the process continues as described above. If the test result in step 712 is YES, indicating that all of the transmit antennas have had their signal contribution processed, control passes to conditional branch point 725, which tests to determine whether one coherence time has elapsed since the previous execution of step 701. If the test result in step 725 is NO, indicating that the channel is believed to still remain substantially the same as when it was last estimated, control passes to step 707, and the process continues as described above. If the test result in step 725 is YES, indicating that sufficient time has passed such that the channel may have changed enough so as not to be considered substantially the same as when it was last estimated, control passes back to step 701 and the process continues as described above.

In an alternative configuration of FIG. 5, switch 533 is connected to the output of an error correction decoder which is either directly or indirectly connected to soft bit mapping 527. Doing so may improve performance.

FIG. 8 shows a particular embodiment of joint equalizer 109, in which the equalization is performed in the discrete frequency domain, in accordance with an aspect of the invention. Shown in FIG. 8 making up joint equalizer 109 are a) fast Fourier transform (FFT) processors 801, including FFT processors 801-1 through 801-N, where N is the number of receive antennas; b) channel estimators 803, including channel estimators 803-1 through 803-N; c) fast Fourier transform (FFT) processors 805, including FFT processors 805-1 through 805-N*M, where M is the number of transmit antennas; d) MMSE detection per frequency bin processor 807; and e) inverse fast Fourier transform (IFFT) processors 809, including IFFT processors 809-1 through 809-M.

Each of FFT processors 801 receives from front-end 107 a signal of time domain digital samples corresponding to a respective one of receive antennas 105-N and performs the FFT algorithm on a set of consecutive samples to convert the time domain samples to samples in the discrete frequency domain, $r_n(\omega)$, where ω is a particular discrete frequency. The number of samples F is at the discretion of the implementer based on a tradeoff between the performance and complexity of FFT processors 801. Typically the number of samples is a power of 2, e.g., 128, although the more samples the more accurate the equalization process will be. The possible values for ω are determined as $\omega = \frac{2\pi n}{T_s F}$, where *n* ranges from 0 to F-1. The resulting discrete frequency samples for each receive antenna are supplied to MMSE detection per frequency bin processor 807.

Each of channel estimators 803 also receives from front-end 107 a signal of time domain digital samples corresponding to a respective one of receive antennas 105-N and performs a channel estimate for the channel between its respective receive antenna and each of the M transmit antennas, thereby producing M channel estimates. Each channel estimate is a series of complex numbers that defines the impulse response of the channel. Fast Fourier transform (FFT) processors 805 each converts a respective channel estimate into the discrete frequency domain representation thereof, and supplies the resulting discrete frequency domain representation of the channel estimates $\mathbf{h}_{n,m}(\omega)$ to MMSE detection per frequency bin processor 807.

MMSE detection per frequency bin processor 807 performs the equalization in the frequency domain by computing

$$\mathbf{z}(\omega)=\left(\mathbf{H}(\omega)^H\,\mathbf{H}(\omega)+\sigma^2\mathbf{I}\right)^{-1}\mathbf{H}(\omega)^H\,\mathbf{r}(\omega) \qquad \text{equation (23)}$$

where

$$\mathbf{H}(\omega)=\begin{bmatrix}\mathbf{h}_{1,1}(\omega) & \cdots & \mathbf{h}_{1,M}(\omega)\\ \vdots & \ddots & \vdots\\ \mathbf{h}_{N,1}(\omega) & \cdots & \mathbf{h}_{N,M}(\omega)\end{bmatrix} \qquad \text{equation (24)}$$

$$\mathbf{r}(\omega)=\begin{bmatrix}\mathbf{r}_1(\omega)\\ \mathbf{r}_2(\omega)\\ \vdots\\ \mathbf{r}_N(\omega)\end{bmatrix} \qquad \text{equation (25)}$$

$$\sigma^2=\frac{\sigma_n^2}{\sigma_x^2}, \qquad \text{equation (26)}$$

σ_n^2 is the background noise plus interference power,

σ_x^2 is the power of the downlink signal from the base station to the terminal, and

I is the identity matrix.

Each of the resulting M components of resulting vector $\mathbf{z}(\omega)$ are then inverse frequency transformed from the discrete frequency domain into the time domain by inverse fast Fourier transform (IFFT) processors 809. The time domain equalized outputs are then supplied as the output of joint equalizer 109.

FIG. 9 shows a particular embodiment of joint equalizer 109 in which the equalization is calculated in the discrete frequency domain and applied in the time domain, in accordance with an aspect of the invention. Shown in FIG. 9 making up joint equalizer

109 are a) matrix finite impulse response (FIR) filter 901; b) channel estimators 903, including channel estimators 903-1 through 903-N; c) fast Fourier transform (FFT) processors 905, including FFT processors 905-1 through 905-N*M, where M is the number of transmit antennas; d) MMSE tap weight calculator 907; and e) inverse fast Fourier transform (IFFT) processors 909, including IFFT processors 909-1 through 909-N*M

Matrix finite impulse response (FIR) filter 901 continuously receives from front-end 107 a signal of time domain digital samples corresponding to a respective one of receive antennas 105-N. The number of taps of matrix FIR filter 901 is at the discretion of the implementer based on a tradeoff between performance and complexity. Typically the number of samples is a power of 2, e.g., 128.

Each of channel estimators 903 also receives from front-end 107 a signal of time domain digital samples corresponding to a respective one of receive antennas 105-N and performs a channel estimate for the channel between its respective receive antenna and each of the M transmit antennas, thereby producing M channel estimates. Each channel estimate is a series of complex numbers that defines the impulse response of the channel. Fast Fourier transform (FFT) processors 905 each converts a respective channel estimate into the discrete frequency domain, and supplies the resulting discrete frequency domain representation of the channel estimates $\mathbf{h}_{n,m}(\omega)$ to MMSE tap weight calculator 907. The number of samples employed by FFT processors 905 for each conversion should be the same as the number of taps in matrix FIR filter 901.

MMSE tap weight calculator 907 develops frequency domain representations of the weights necessary to perform the equalization in the time domain by computing

$$\mathbf{S}(\omega)=\left(\mathbf{H}(\omega)^{H}\,\mathbf{H}(\omega)+\sigma^{2}\mathbf{I}\right)^{-1}\mathbf{H}(\omega)^{H} \qquad \text{equation (27)}$$

where $\mathbf{H}(\omega)$, σ^2 are defined as explained hereinabove in connection with FIG. 8.

Each of the resulting M components of resulting vector $\mathbf{S}(\omega)$ are grouped by frequency into frequency vectors, and are then the frequency vectors are inverse frequency transformed from the discrete frequency domain to become filter weights in the time domain by inverse fast Fourier transform (IFFT) processors 909. The weights are then supplied to matrix FIR filter 901 which utilizes them to perform equalization in the time domain on the signals received from front-end 107 as shown by equation 28,

$$\mathbf{y}(k)=\sum_{j=0}^{F-1}\mathbf{S}_{j}\mathbf{r}(k-j) \qquad \text{equation (28)}$$

where $\mathbf{y}(k)$ is the vector output at time k, $\mathbf{y}$ having M components—one for each transmit antenna—, $\mathbf{S}_j$ is the MxN filter matrix for delay j, which is the inverse Fourier transform of $\mathbf{S}(\omega)$, $\mathbf{r}(k)$ is the vector input signal which is received by matrix FIR filter 901 as defined in equation (9), and F is the number of samples taken for each FFT.

Given the foregoing, those of ordinary skill in the art will readily recognize that other equalizer algorithms which approximate the operation and performance of MMSE, such as least mean square (LMS), recursive least squares (RLS), or minimum intersymbol interference (ISI) subject to an anchor condition, can be employed in a joint manner, e.g., in a space manner, in the implementation of joint equalizer 109.

Those of ordinary skill in the art will readily recognize that the techniques of the instant invention may be employed in systems in which the various transmit antennas are transmitting at different data rates, e.g., using different encoding rates and/or transmit constellations, such as quaternary phase-shift keying (QPSK) or 16-ary quadrature amplitude modulation (16-QAM). In such a situation, if the embodiment of FIG. 5 is employed, order controller 531 is not required because the antennas must always be processed in an a priorily determined order.